# IPXOGF22 Datasheet

## Low-Power XTAL Oscillator IP in GLOBALFOUNDRIES 22FDX

## 1. Features

- Low Power Consumption
- Low Phase Noise
- On-Chip Tuning Capacitor Bank
- Wide operating voltage range: 1V to 1.98V
- Single-Supply Voltage Operation
- Wide Operating Temperature: -40°C to 125°C
- ESD Protection

## 2. Applications

- Frequency Synthesizers
- Wireless and Wired communications
- Portable and Battery-Operated Devices
- Microcontroller Clock
- Power Management

## 3. General Description

The IPXOGF22 is a silicon-proven ultra-low power Crystal Oscillator (XO) with amplitude detector. The amplitude detector together with synchronizers at output buffer guarantee a glitch-free square-wave at the output. The circuit structure of this IP offers low current consumption and low complexity. The oscillator core is optimized to provide the largest oscillation amplitude and the lowest phase noise with based on the provided bias current. The IP has several programmability options and supports a wide range of crystals with different ESR values.

The IP is compatible with all *_2Mx_4Cx_1Ix_* metal stack options. This means metal stacks #14, #16, and #17 readily compatible. For metal stacks #3, #8, #,11, #19, #21, and #22 minor layout modification should be done by the supplier. For other metal stacks, please contact the supplier.

## Contact Information


| | |
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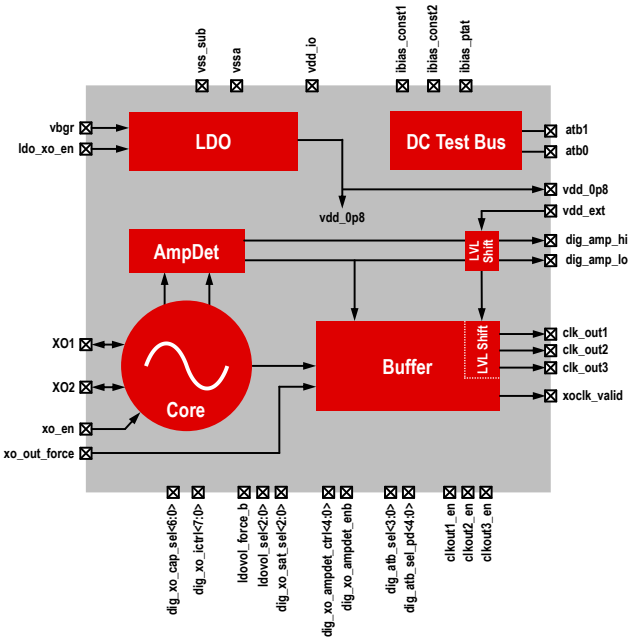


*Figure 1. Functional Block Diagram*

# 4. Table of Contents



# 5. Revision History

Revision 1.51: Jan 2021

- Adding detailed specifications

Revision 1.00: initial version (Nov 2020)

- Initial version

# 6. Pin Configuration and Functions

*Table 1. Pin Configuration and Functions*

| Pin Name | Metal Layer | Type | Power Domain | Description |
|---|---|---|---|---|
| **Signal Plane** | | | | |
| XO1 | IA | Analog In/Out | $V_{DD\_CORE}$ | XTAL connection pin #1; input clock for external mode |
| XO2 | IA | Analog In/Out | $V_{DD\_CORE}$ | XTAL connection pin #2 |
| clk_out1 | M2 | Digital Output | $V_{DD\_EXT}$ | Digital output clock signal #1 |
| clk_out2 | M2 | Digital Output | $V_{DD\_EXT}$ | Digital output clock signal #2 |
| clk_out3 | M2 | Digital Output | $V_{DD\_EXT}$ | Digital output clock signal #3 |
| xoclk_valid | M2 | Digital Output | $V_{DD\_IO}$ | Valid flag of output clock |
| atb0 | C3 | Analog Output | $V_{DD\_IO}$ | DC analog test bus 0, for monitoring vbgr_0p8 and v_ptat |
| atb1 | M2 | Analog Output | $V_{DD\_IO}$ | DC analog test bus 1, for monitoring LDO signals |
| **Control Plane** | | | | |
| ldo_xo_en | M2 | Digital Input | $V_{DD\_IO}$ | LDO enable control |
| ldovol_sel<2:0> | M2 | Digital Input | $V_{DD\_IO}$ | Internal LDO overdrive voltage select control, from 800mV (default) to 960mV |
| ldovol_force_b | M2 | Digital Input | $V_{DD\_IO}$ | Force LDO overdrive voltage to default (active low) |
| dig_xo_sat_sel<2:0> | M2 | Digital Input | $V_{DD\_IO}$ | LDO number of satellites select control (thermometer code) |
| xo_en | M2 | Digital Input | $V_{DD\_IO}$ | XO core enable |
| dig_xo_cap_sel<6:0> | M2 | Digital Input | $V_{DD\_IO}$ | XO core capacitor control |
| dig_xo_ictrl<7:0> | M2 | Digital Input | $V_{DD\_EXT}$ | XO core current control |
| clkout1_en | C2 | Digital Input | $V_{DD\_EXT}$ | Enable output clock #1 |
| clkout2_en | C2 | Digital Input | $V_{DD\_EXT}$ | Enable output clock #2 |
| clkout3_en | C2 | Digital Input | $V_{DD\_EXT}$ | Enable output clock #3 |
| dig_xo_ampdet_ctrl<4:0> | M2 | Digital Input | $V_{DD\_EXT}$ | AmpDet window control (from 0 to 17) |
| dig_xo_ampdet_enb | C2 | Digital Input | $V_{DD\_EXT}$ | AmpDet enable (active low) |
| dig_amp_hi | C3 | Digital Output | $V_{DD\_EXT}$ | AmpDet window-high comparator output |
| dig_amp_lo | C3 | Digital Output | $V_{DD\_EXT}$ | AmpDet window-low comparator output |
| dig_atb_sel_pd<4:0> | M2 | Digital Input | $V_{DD\_IO}$ | atb0 multiplexer select pins. Only one of the pins should be high (one-hot code) |
| dig_atb_sel<3:0> | M2 | Digital Input | $V_{DD\_IO}$ | atb1 multiplexer select pins. Only one of the pins should be high (one-hot code) |
| **Power Plane** | | | | |
| vdd_io | IA | Analog Power | $V_{DD\_IO}$ | Main supply pin. Recommended to be directly connected to analog supply pad of the chip at top-level (star-connect) |
| vdd_ext | IA | Digital Power | $V_{DD\_EXT}$ | External supply voltage 0.8V |
| vssa | IA | Analog Ground | GND | Main ground pin. Recommended to be directly connected to analog ground pad of the chip at top-level (star-connect) |
| vss_sub | IA | Substrate Ground | GND | Substrate ground pin. Recommended to be directly connected to analog ground pad of the chip at top-level (star-connect) |
| vbgr | C4 | Analog Input | $V_{DD\_IO}$ | Input reference voltage 0.8V |

| Pin Name | Metal Layer | Type | Power Domain | Description |
|---|---|---|---|---|
| ibias_const1 | C3 | Analog Input | $V_{DD\_IO}$ | LDO reference bias sink current 0.5µA |
| ibias_const2 | M2 | Analog Input | $V_{DD\_CORE}$ | Oscillator Core reference bias sink current 1µA |
| ibias_ptat | C3 | Analog Input | $V_{DD\_CORE}$ | AmpDet PTAT bias sink current 1µA |

## 7. Dimensions

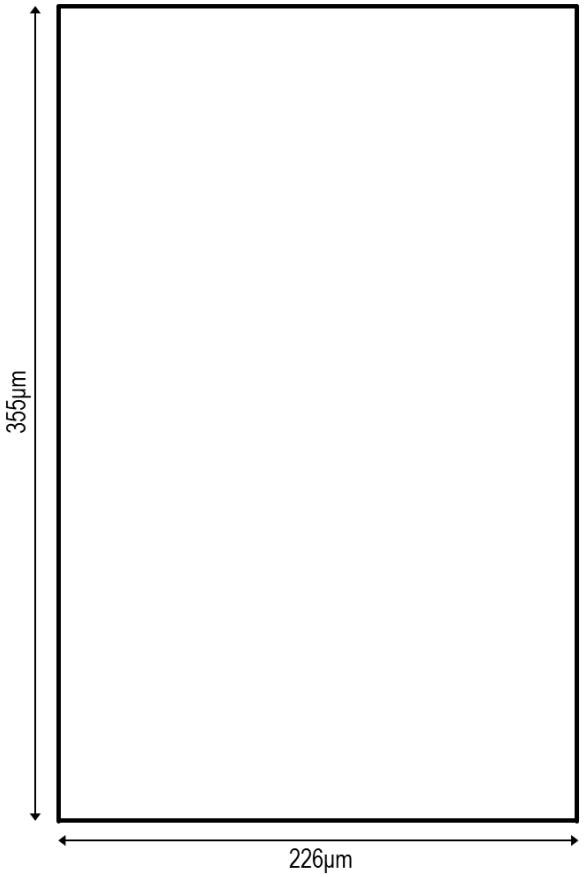


*Figure 2. Dimensions Overview*

# 8. Specifications

## 8.1. Electrical Characteristics

### 8.1.1. Operating Conditions

$T_J$ = 27°C, all typical voltages and currents, default settings and crystal as specified in Error! Reference source not found. and Error! Reference source not found., unless otherwise noted.

*Table 2. Operating Conditions*

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Main Supply Voltage | $V_{DD\_IO}$ | | 1 | 1.8 | 1.98 | V |
| External Core Supply Voltage | $V_{DD\_EXT}$ | | 0.72 | 0.8 | 0.88 | V |
| Internal Core Supply Voltage | $V_{DD\_CORE}$ | Vref=0.8V | 0.785 | 0.8 | 0.815 | V |
| Input Reference Voltage | $V_{REF}$ | | 0.76 | 0.8 | 0.84 | V |
| LDO Input Reference Bias Current | $I_{REF1}$ | | 0.375 | 0.5 | 0.625 | µA |
| XO Core Input Reference Bias Current | $I_{REF2}$ | | 0.75 | 1 | 1.25 | µA |
| AmpDet Input PTAT Bias Current | $I_{PTAT}$ | PTAT @ 27°C | 0.75 | 1 | 1.25 | µA |
| Operating Temperature | $T_J$ | | -40 | 27 | 125 | °C |
| LDO Boost Level | $\Delta V_{DD}$/code | | | 40 | | mV/code |
| Supply Current<br>All Blocks Enabled<br>All Blocks Disabled | $I_{DD\_IO}$ | Default settings | | <br>175<br>8.9 | | <br>µA<br>nA |
| Input High Voltage on $V_{DD\_IO}$ Domain | $V_{IH\_IO}$ | | 0.7x$V_{DD_IO}$ | | | |
| Input Low Voltage on $V_{DD\_IO}$ Domain | $V_{IL\_IO}$ | | | | 0.3x$V_{DD_IO}$ | |
| Input High Voltage on $V_{DD\_EXT}$ Domain | $V_{IH\_EXT}$ | | 0.7x$V_{DD_EXT}$ | | | |
| Input Low Voltage on $V_{DD\_EXT}$ Domain | $V_{IL\_EXT}$ | | | | 0.3x$V_{DD_EXT}$ | |
| ATB Mux On-State Resistance[1] | $R_{ON}$ | $T_J$ = 27°C, atb voltage 0V to 0.95V | | | 50 | kΩ |
| ATB Mux Off-State Leakage to Ground[1] | $I_{L\_OFF}$ | $T_J$ = 27°C, atb voltage 0V to 0.95V | | | 200 | pA |

[1] Each unit of ATB's analog multiplexer.

### 8.1.2. Oscillator Characteristics

$T_J$ = 27°C, all typical voltages and currents, default settings and crystal as specified in **Error! Reference source not found.** and **Error! Reference source not found.**, unless otherwise noted.

*Table 3. Electrical Characteristics of Output Voltages*

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation Frequency | $f_{OSC}$ | | 10 | 24 | 52 | MHz |
| On-Chip Tunable Capacitance | $C_{TUNE}$ | Single-ended, 7-bits | 1.8 | | 31.3 | pF |
| Oscillator Core Transconductance | $g_m$ | | | 4.16 | | ms |
| Oscillation Amplitude | $V_{OSC}$ | Single-ended peak | | 400 | | mV |
| Startup Time | $t_{STARTUP}$ | | | 2.1 | | msec |
| Duty Cycle | DCY | | 47 | 50 | 53 | % |
| Frequency Drift[1] | Δf/ΔT | Excluding XTAL drift | | 0.006 | | ppm/°C |
| Output Rise Time | $t_r$ | Output load cap = 17fF | | 173 | | ps |
| Output Fall Time | $t_f$ | Output load cap = 17fF | | 125 | | ps |
| Phase Noise 24MHz | PN | ictrl=170 (default setting) | | | | |
| | | @ 10Hz | | -72 | | dBc/Hz |
| | | @ 100Hz | | -103 | | dBc/Hz |
| | | @ 1kHz | | -124 | | dBc/Hz |
| | | @ 10kHz | | -132 | | dBc/Hz |
| | | @ 100kHz | | -136 | | dBc/Hz |
| Phase Noise 24MHz | PN | ictrl=50 (optimum setting[2]) | | | | |
| | | @ 10Hz | | -97 | | dBc/Hz |
| | | @ 100Hz | | -112 | | dBc/Hz |
| | | @ 1kHz | | -122 | | dBc/Hz |
| | | @ 10kHz | | -128 | | dBc/Hz |
| | | @ 100kHz | | -131 | | dBc/Hz |

[1] Coefficient specified by "box method": The upper and lower current extremes measured over temperature define the top and bottom of the box. The sides are determined by the specified temperature range of the device. The drift of the unit is the slope of the diagonal.

[2] Optimized for long-term jitter.

### 8.1.3. Amplitude Detector

$T_J$ = 27°C, all typical voltages and currents, unless otherwise noted.

*Table 4. Electrical Characteristics of Output Voltages*

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Detection Window Size | $V_{WIN}$ | | | 22.5 | | mV |
| Detection Range | $V_{DET}$ | Single-ended peak | 42 | | 444 | mV |
| Amplitude Detection accuracy | $\Delta V_{DET}$ | | -10 | | +10 | mV |
| Supply Current | $I_{AmDet}$ | | | 2.5 | | µA |

## 8.2. Typical Characteristics

$T_J$ = 27°C, all typical voltages and currents, default settings and typical crystal as specified in **Error! Reference source not found.** and **Error! Reference source not found.**, unless otherwise noted.

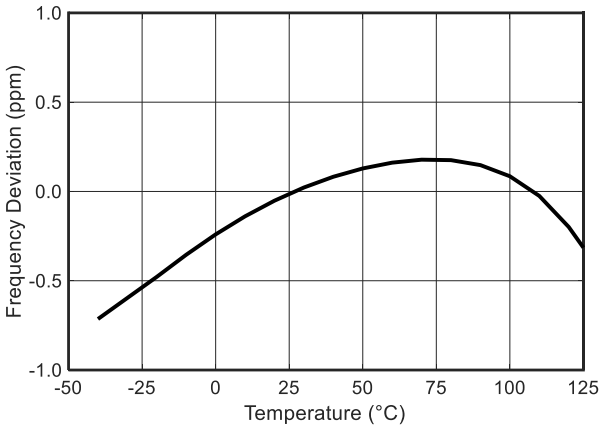


*Figure 3. Frequency Error vs Temperature*

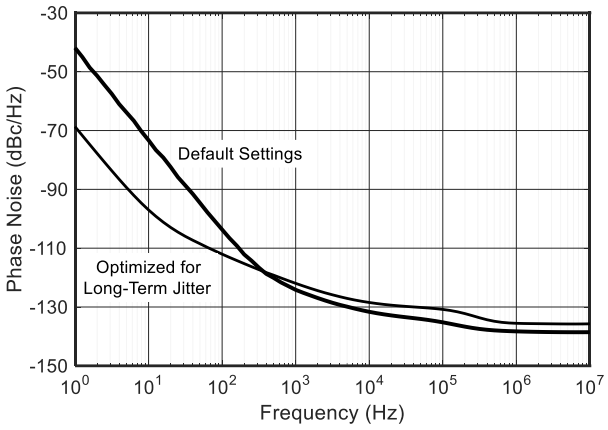


*Figure 4. Output Phase Noise Spectrum*

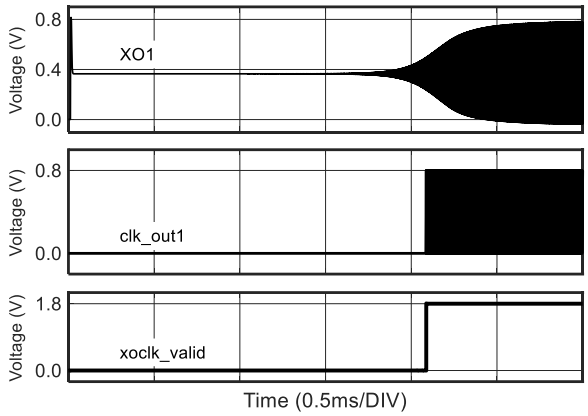


*Figure 5. Startup Settling for the Default XTAL*

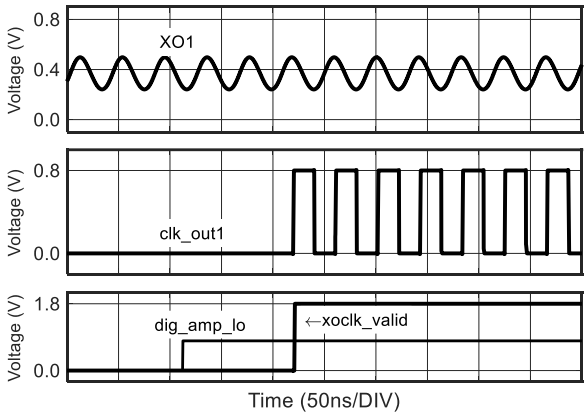


*Figure 6. Startup Settling for the Default XTAL (Zoom-in).*

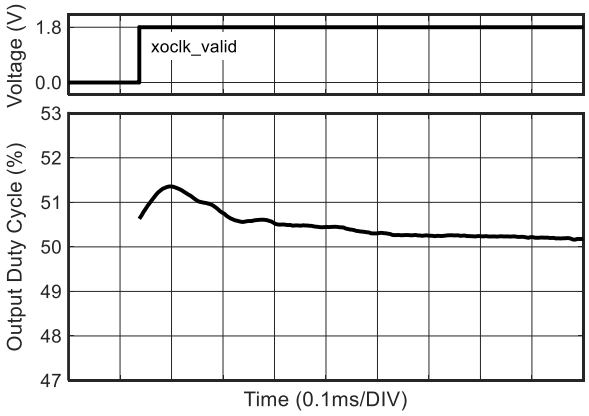


*Figure 7. Output Duty Cycle vs Time for the Default XTAL*

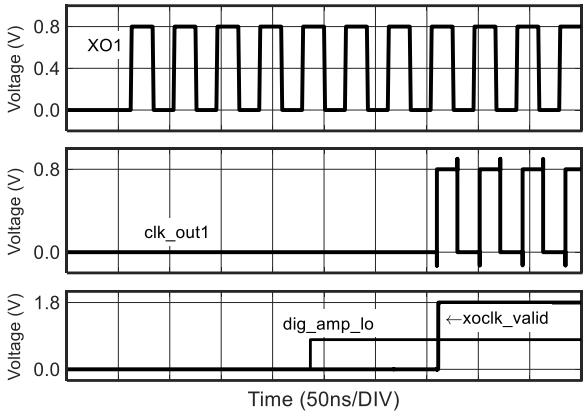


*Figure 8. External Mode Startup*

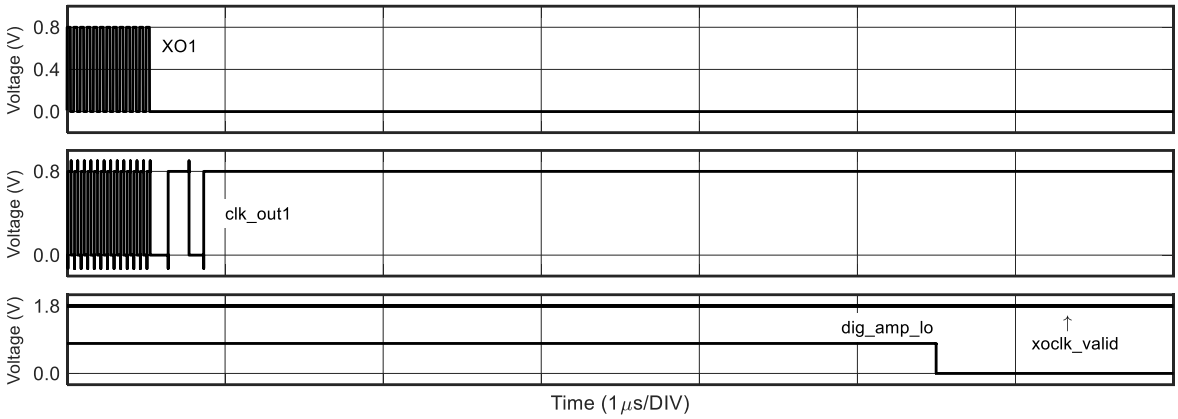


*Figure 9. External Mode Stopping*

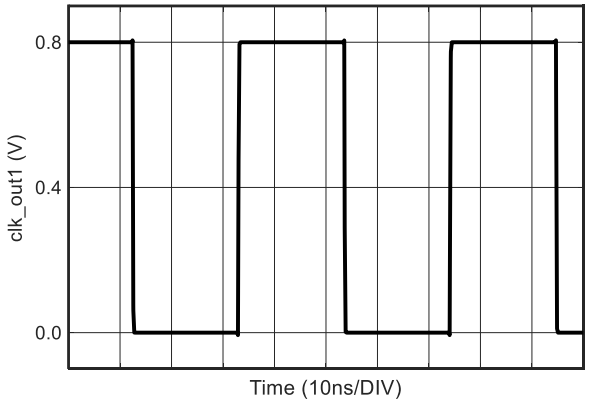


*Figure 10. Typical Output Waveform*

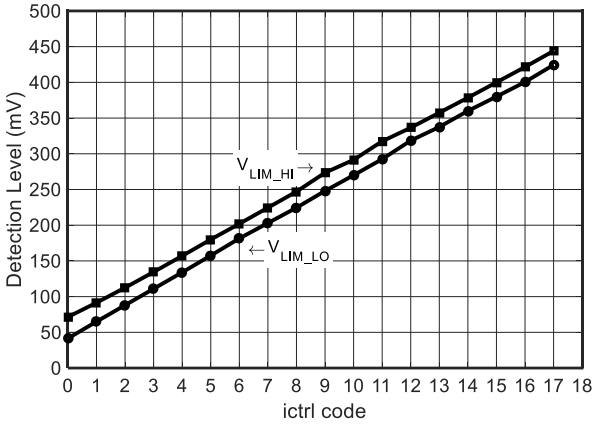


*Figure 11. Amplitude Detector Characteristic*

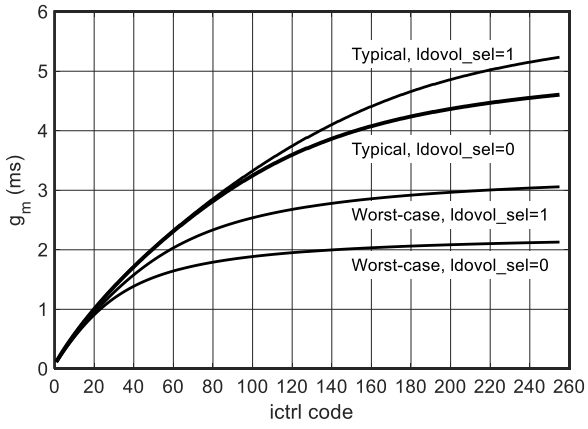


*Figure 12. Oscillator Core $g_m$ vs ictrl Code*

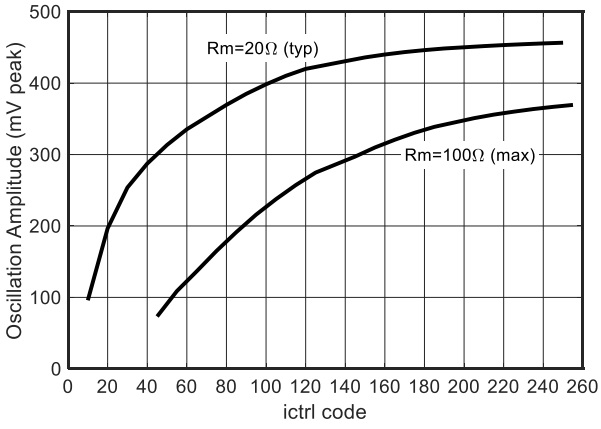


*Figure 13. Oscillation Amplitude vs ictrl Code*

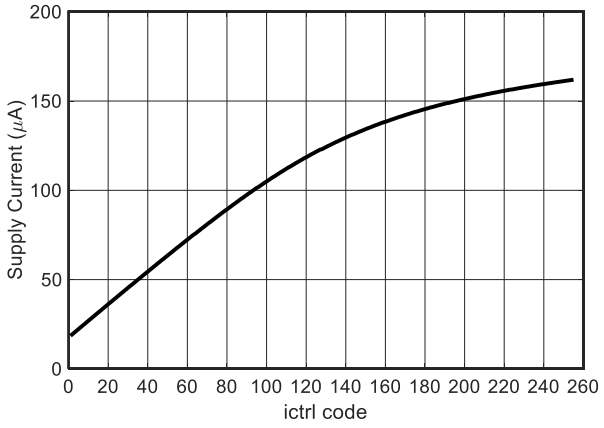


*Figure 14. Current vs ictrl code*

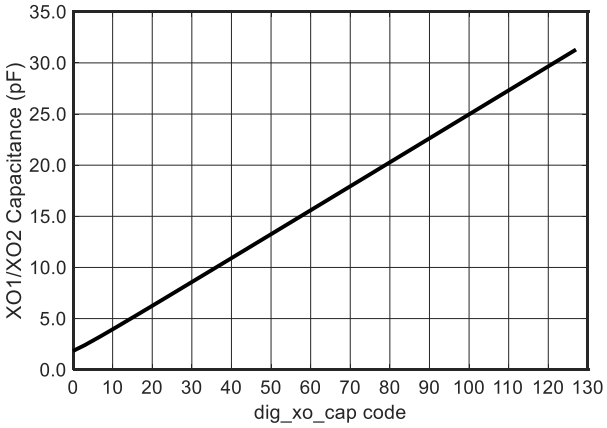


*Figure 15. Load Cap vs cap_ctrl code*